RAMSEY Chip Specification

Description

This specification describes the requirements for an integrated circuit which is a custom gate array designed to function mainly as a dynamic RAM controller. The device, called RAMSEY, allows the 68030 chip to interface with up to 16 megabytes of system DRAM. RAMSEY also contains logic associated with the DMAC controller (super DMAC).

Some of the key features of RAMSEY are:

- Four megabytes of memory using 32 standard 256K x 4 DRAMs (80 ns)
- Sixteen megabytes of memory using 32 standard 1M x 4 DRAMs (80 ns)
- Support of 68030 burst mode (requires 80 ns static column DRAMs)
- Page mode RAM access (requires 80 ns static column DRAMs)
- Automatic CAS-before-RAS refreshing of DRAMs
- Multiplexing of addresses

Configuration

The device shall be configured as a standard 84-pin PLCC. Refer to Figure 6-14 for pin configuration. Refer to Figures 6-15 through 6-20 for timing diagrams.

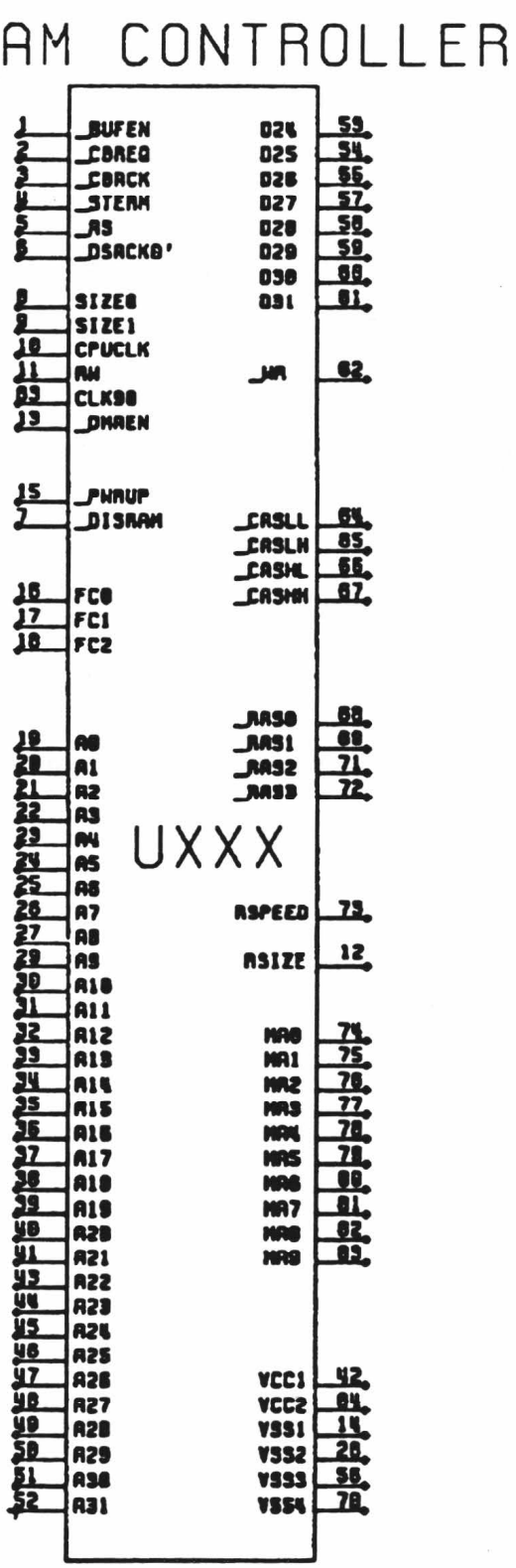

Figure 6-14. Pin Configuration

Sources

Refer to *Approved Vendors List* on page 6-58.

Pin Description

Name	Dir	Description
D24-D31	Bi	Data signals from/to 68030.
A0-A31	Bi	Address inputs from 68030. Become outputs when *DMAEN is valid.
FC0-FC2	Bi	Function code inputs from 68030. Outputs when *DMAEN is valid.
RW	Bi	Read/write input from 68030. Output when *DMAEN is valid.
SIZE0,1	Bi	Function code inputs from 68030. Outputs when *DMAEN is valid.
*AS	Input	Address strobe input.
CBREQ	Input	Cache burst request from 68030.
*CBACK	Output	Cache burst acknowledge. Tri-state output that is turned on when the RAM address space is decoded.
*STERM	Bi	Synchronous termination. Output during RAM access. Input when *DMAEN is valid. Tri-state output that is turned on when the RAM address space is decoded.
*PWRUP	Input	Powerup input. When valid, the internal register is restored to its default values.
*DISRAM	Input	Disable RAM. When valid, internal decoding of the RAM address space is disabled.
*DMAEN	Input	DMA enable. Input from onboard DMAC indicating that it is now the bus master.
*DSACK0	Bi	Data size and acknowledge (bit 0) output to 68030 (open collector). Input when *DMAEN is valid.
CPUCLK	Input	System clock.
CLK90	Input	System clock delayed 90 degrees.
*BUFEN	Output	Buffer enable. Output enable signal for 74F245s which tie the local RAM data bus to the system's data bus.
*WR	Output	Write signal to the DRAMs.
*CASxx	Output	Column address strobes to the RAMs.
*RASx	Output	Row address strobes to the RAMs.
RSPEED	Input	RAM speed. When high, the RAM controller assumes a 25 MHz system. If low, assumes 16 MHz operation.
RSIZE	Input	RAM size. If low, assumes the RAMs are 256K x 4. If high, assumes they are 1M x 4.
MA0-MA9	Output	Multiplexed address bits to DRAMs.

Note For -07 only, the following pins have a TTL Vih min. of 2.4. These values supersede documents dated before March 17, 1992.

Signal Name	Pin	Signal Name	Pin
DISRAM_I_	7	RSIZE_I	12
SIZE1	9	OWN_	13
CPUCLK_I	10	CLK90_I	63
RW_1	11	SPEED	73

Operation

RAMSEY Control Register

There is a single 8-bit register internal to RAMSEY which can be used to change its mode of operation. This register is readable and writable. It is located at $00DE0003 of the supervisor data space. Data written into the register does not take effect until the next refresh occurs. Consequently, if you write a value to the register you will have to wait out the refresh interval before the value can be read back. Each of these bits has a default value that it is set to when the *PWRUP bit is low.

bit 0	Page Mode	When high, page mode is enabled (default=0).
bit 1	Burst Mode	When high, RAMSEY will respond to the *CBREQ input and do burst cycles (default=0).
bit 2	Wrap	If high, all 4 longwords of a burst will be allowed to take place. If Wrap is disabled, then the burst will only continue while A3,A2 are increasing. Bursts will not be allowed to wrap to A3,A2=00 (default=0).
bit 3	RAMsize	If low, then RAM is 1 megabit (256K x 4 or 1M x 1). If high, then RAM is 4 megabit (1M x 4). The default value is determined by the RSIZE input.
bit 4	RAMwidth	For -04 only, if low, then RAM is 1 bit wide (1M x 1). If high, then RAM is 4 bits wide (256K x 4 or 1M x 4) (default=1).
bit 4	Skip	For -07 only, if set high, then RAM is accessed in 4 clocks, instead of 5 (25 MHz). S11 in timing diagrams is omitted. This requires VERY fast DRAMs (default = 0).
bit 5,6	Refresh Rate	The refresh counter uses the CPUCLK to count out refresh times. The number of clocks between refreshes is determined by the following table:

		Refresh Interval (μsecs)	
Bit 6,5	# of Clocks	16 MHz	25 MHz
00	154	9.24	6.16
01	238	14.28	9.52
10	380	22.8	15.2
11	oo	(refresh turned off)	

Since 512 refreshes must be done in 8 msecs, the interval between refreshes must be less than 15.625 μsecs. During page mode, RAS can only be low for 10 μsecs at a time, so the refresh rate should be set to less than 10 μsecs when page mode is enabled. The default values are determined by the RSPEED input. If RSPEED is low, then the default value for bits 6,5=00. If RSPEED is high, then the default for bits 6,5=01.

bit 7 TEST This bit is used for testing only.

Version Register

There is a read only register at $00DE0043 that contains the version number of the RAMSEY chip.

-04 (12D) RAMSEY returns a version number of $0D.

-07 (12G) RAMSEY returns a version number of $0F.

RAM Memory Map

$07C00000 - $07CFFFFF RAS0
$07D00000 - $07DFFFFF RAS1
$07E00000 - $07EFFFFF RAS2
$07F00000 - $07FFFFFF RAS3
RSIZE=0, RAMWIDTH=1

$07000000 - $073FFFFF RAS0
$07400000 - $077FFFFF RAS1
$07800000 - $07BFFFFF RAS2
$07C00000 - $07FFFFFF RAS3
RSIZE=1, RAMWIDTH=1

$07C00000 - $07FFFFFF RAS0
RSIZE=0, RAMWIDTH=0

RAM Controller Description

RAMSEY is designed to work at two system speeds: 16.67 MHz and 25 MHz. The RSPEED input tells RAMSEY which speed the system is using.

In an effort to improve overall system performance, RAMSEY has several different modes of operation. The two basic modes of operation are referred to as standard and page. Both standard and page modes can be run with or without burst mode, and burst mode can be done with or without burst wrap enabled.

Standard Mode

In this type of operation both page mode and burst mode are disabled. This mode requires standard 80 ns page mode DRAMs. Access to the RAMs always takes five cycles at 25 MHz and four cycles at 16 MHz.

Page Mode

This mode requires 80 ns static column mode DRAMs. When the RAM is accessed, RAS is held low after the cycle completes. This leaves the current RAM 'page' open. While RAS is low, the RAM behaves like a static RAM. Any data within the current page can be accessed by changing the column addresses only. Since the column access time (t_{AA}) is much less than the RAS access time (t_{RAC}), subsequent access to this page of data can be done faster. As long as RAS is held low (10 μsecs max) RAMSEY will allow the CPU to access RAM on this page in only three cycles (16 and 25 MHz).

Comparators inside RAMSEY monitor the ROW address of RAM accesses. If a page is currently open and the ROW address matches (page hit), the RAM can be read in three cycles. If the comparators detect that the data being requested is on a different page (page miss), then RAS must be cycled high and low again, opening up a new page in RAM. Since RAS must be cycled high when a page miss occurs, RAM access takes longer (seven cycles at 25 MHz, five at 16 MHz).

There is some difference in how page mode is done at 16 MHz versus 25 MHz. At 25 MHz, the page comparator only detects page misses when *AS is low and RAM is being accessed. Therefore, when a page is opened (RAS held low), it will remain open until the next refresh occurs, or a page miss is detected. At 16 MHz, however, the page comparator will detect a page miss while *AS is high. Therefore, at 16 MHz a page will only stay open as long as consecutive bus cycles access RAM in this page (or a refresh occurs). At 25 MHz the page will remain open even if bus cycles in between accesses to the currently opened page occur (such as chip memory, CIAs, etc.). This is done so that page misses at 16 MHz will only take five cycles — addresses are valid 1/2 cycle before *AS (30 ns). If it waited until *AS was valid before detecting a page miss, the RAS precharge requirement (t_{RP}) could not be met in 5 cycles.

Burst Mode

This mode requires 80 ns static column DRAMs. In this mode, RAMSEY will respond to the *CBREQ input from the 68030 and allow burst access to RAM. Burst cycles take two clocks each.

Burst Wrapping

The WRAP bit in the RAMSEY control register is associated with burst mode. The 68030 will always request four longword values during a burst sequence. However, if the initial longword is not aligned on a quad longword (A3,A2 not equal to 0,0), the 68030 will read in data which is behind the first data it asked for. Since it is less likely that this data will be used, the WRAP control bit allows you to prevent the 68030 from doing this. If WRAP is low, then the burst will stop after the data with A3,A2 = 1,1 is accessed. If WRAP is high, then all four longwords will be burst.

Since burst and page modes require the use of static column DRAMs, the system must have some means of determining which type of RAMs it contains. If page or burst modes are turned on 'blindly', the machine could crash. Each 1 megabyte bank of Fast memory must be checked. The proper method of checking for static column DRAMs is the following:

1. Disable all interrupts.
2. Turn page mode on by setting the bit in the RAMSEY control register (read it back until the bit takes effect).
3. Write $5AC35AC3, $AC35AC35, $C35AC35A, $35AC35AC to four consecutive longwords in the same page (to be in the same page, A11-A31 must be the same for all four longwords).
4. Turn page mode off by resetting the bit in RAMSEY (wait for it to take effect).

5. Compare the four longword values with what they were written with. If they are correct, then this bank of RAM has all static column DRAMs.
6. Repeat steps 2 through 5 for each 1 MB bank of Fast memory.
7. Re-enable interrupts.

The code that executes this test must **not** be in Fast RAM. Any access to Fast RAM with page mode turned on could cause corruption if any of the RAMs are not static column type. Also, since a refresh cycle will close the page, writes to the four longwords of RAM **must** be less than 10 μsecs apart.

DMAC Support

RAMSEY contains the address counters used during DMA via the onboard contoller. When *DMAEN becomes low, the address lines become outputs and provide the DMA addresses. The DMA address is incremented on the rising edge of *AS whenever *DMAEN is low. Since DMA to both 32 and 16-bit ports is supported, RAMSEY must monitor how the cycle was terminated so that it can increment the address counter by the appropriate amount. If *STERM transitioned low sometime during the cycle, then the port was 32 bits wide and the address is incremented by four. If *DSACK0 transitions during the DMA bus cycle, then the port was also 32 bits wide (*DSACK0 and *DSACK1 are both set low to terminate an asynchronous 32-bit transfer). If neither signal is seen to transition, then it can be assumed that the cycle was terminated by *DSACK1, indicating that the port was 16 bits wide, and the address is incremented by two.

The address counters are preset before DMA is done by writing to the 32-bit register at location $00DD000C (this register is readable as well). The counter can only be preset to a longword-aligned boundary (bits 1 and 0 are always written as 0,0).

-04 The counter can only be preset to an even longword boundary (bits 1 and 0 are always written as 0,0).

-07 The counter can only be preset to an even word boundary (bit 0 is always written as 0). If A1 is high when a cycle terminates, the address is always incremented by 2 regardless of how the cycle terminates.

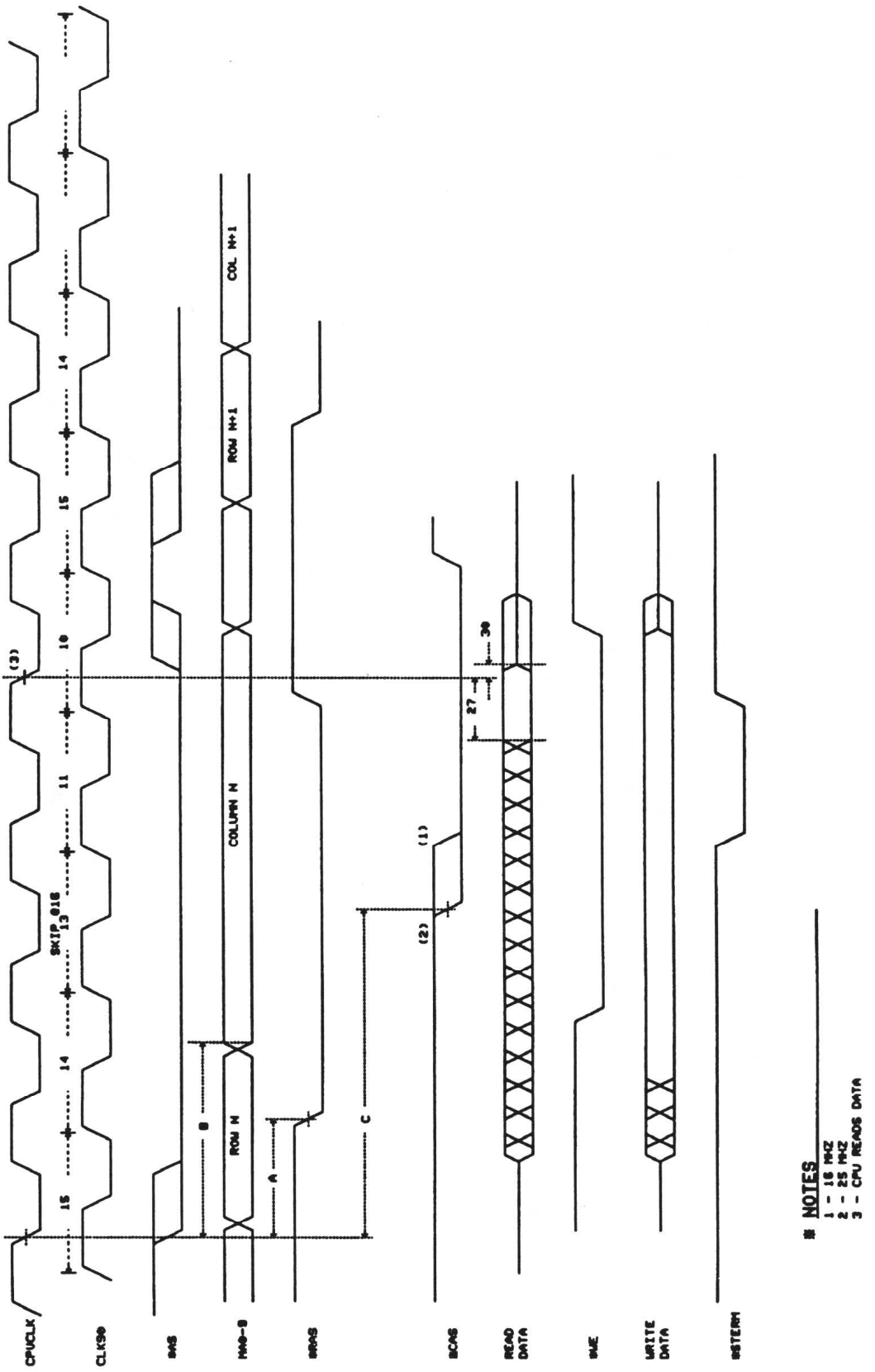

Figure 6-15. Standard RAM Access Timing Diagram (Page Mode Off)

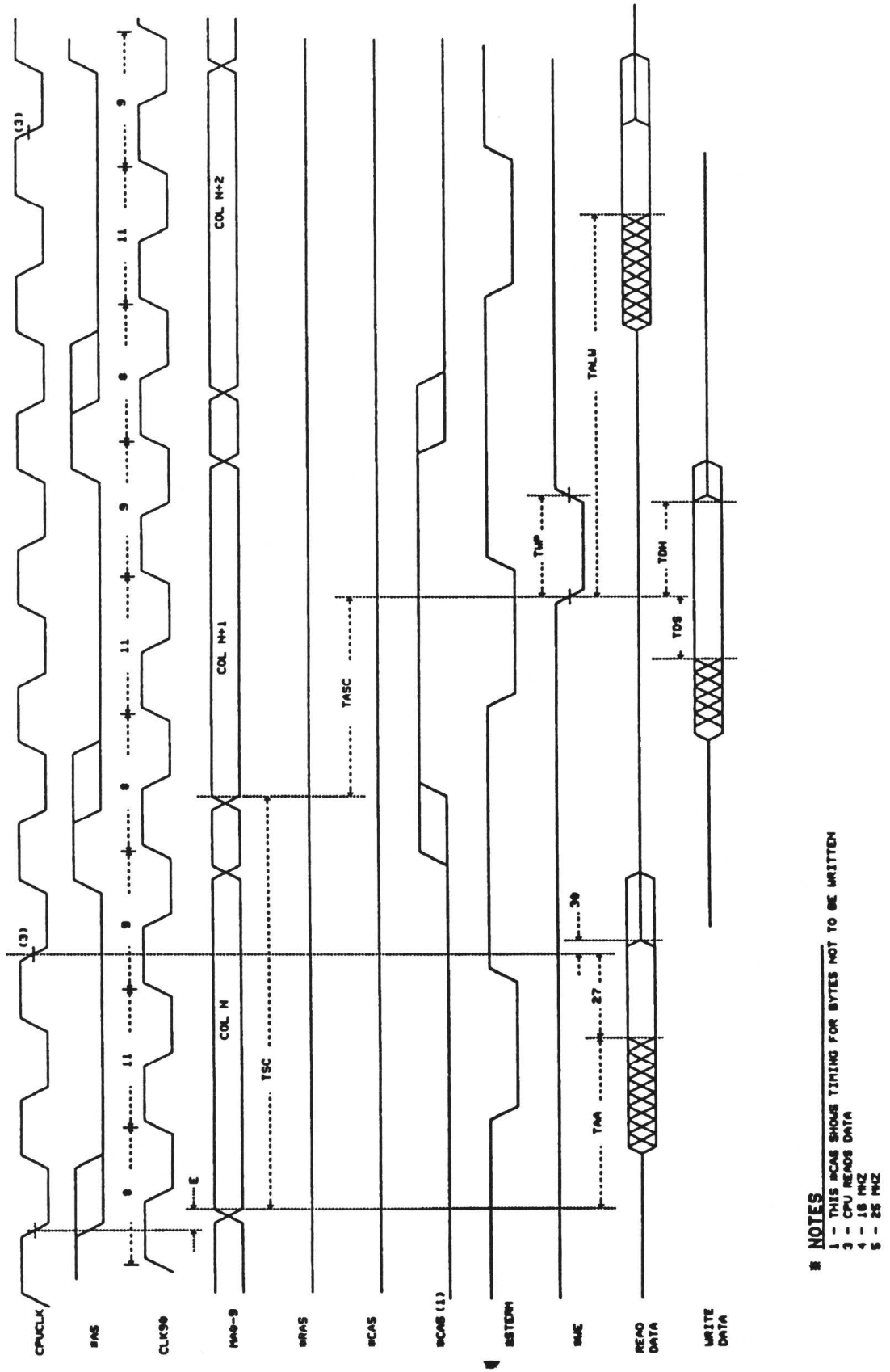

Figure 6-16. RAM Access Timing Diagram (Page Hit, Mixed Read/Write)

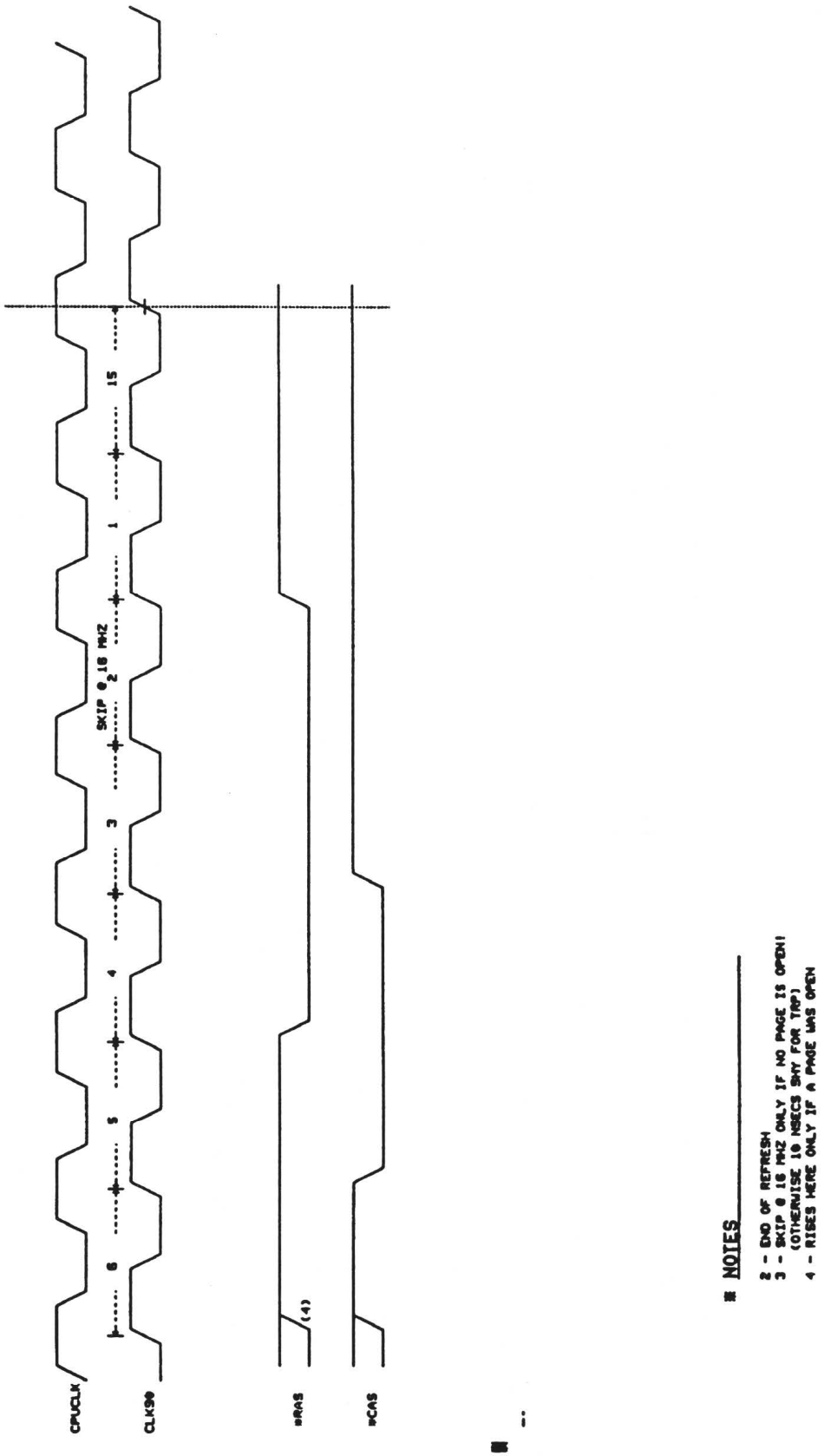

Figure 6-17. Refresh Timing Diagram

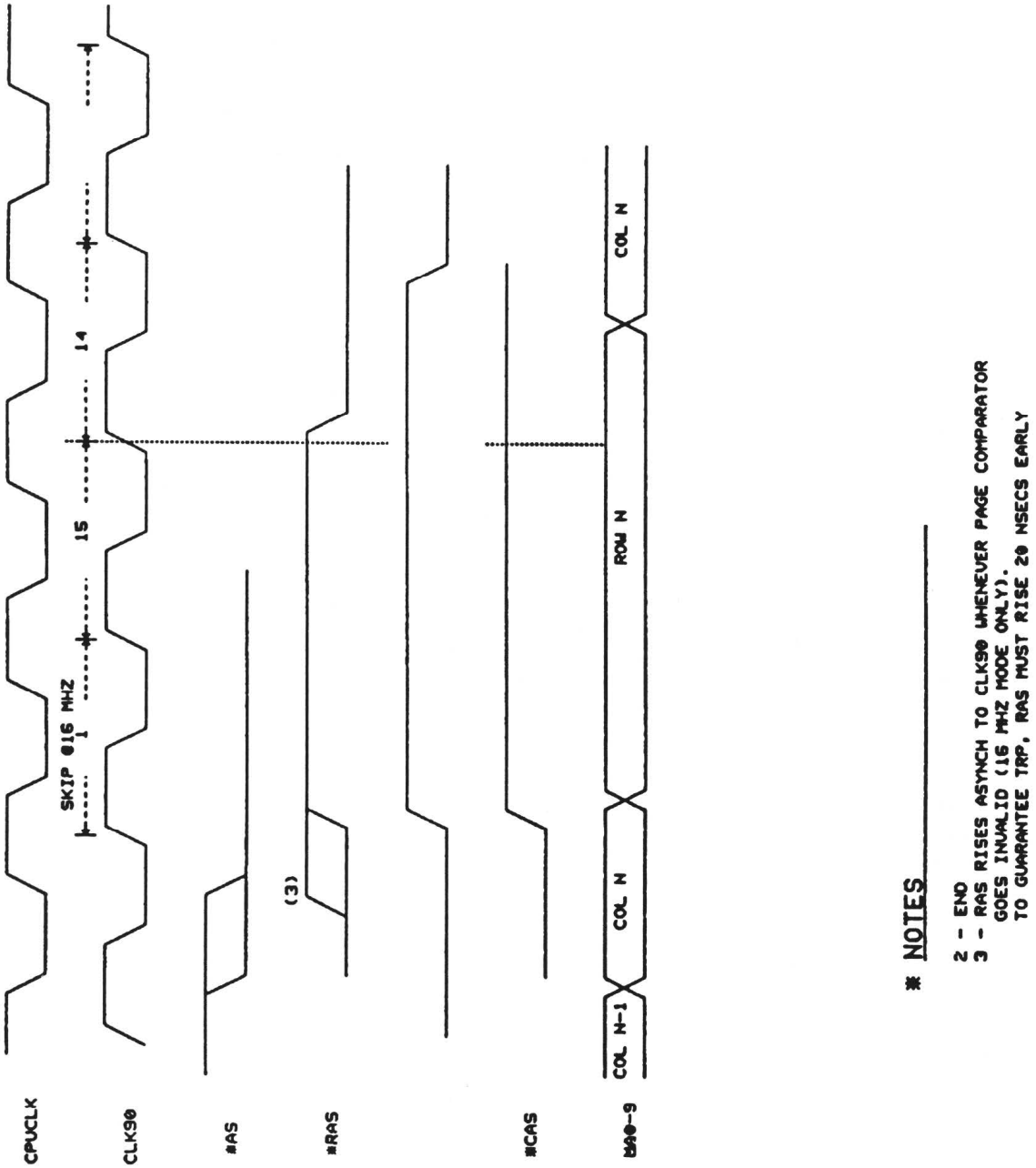

Figure 6-18. Timing Diagram for Closing a Page

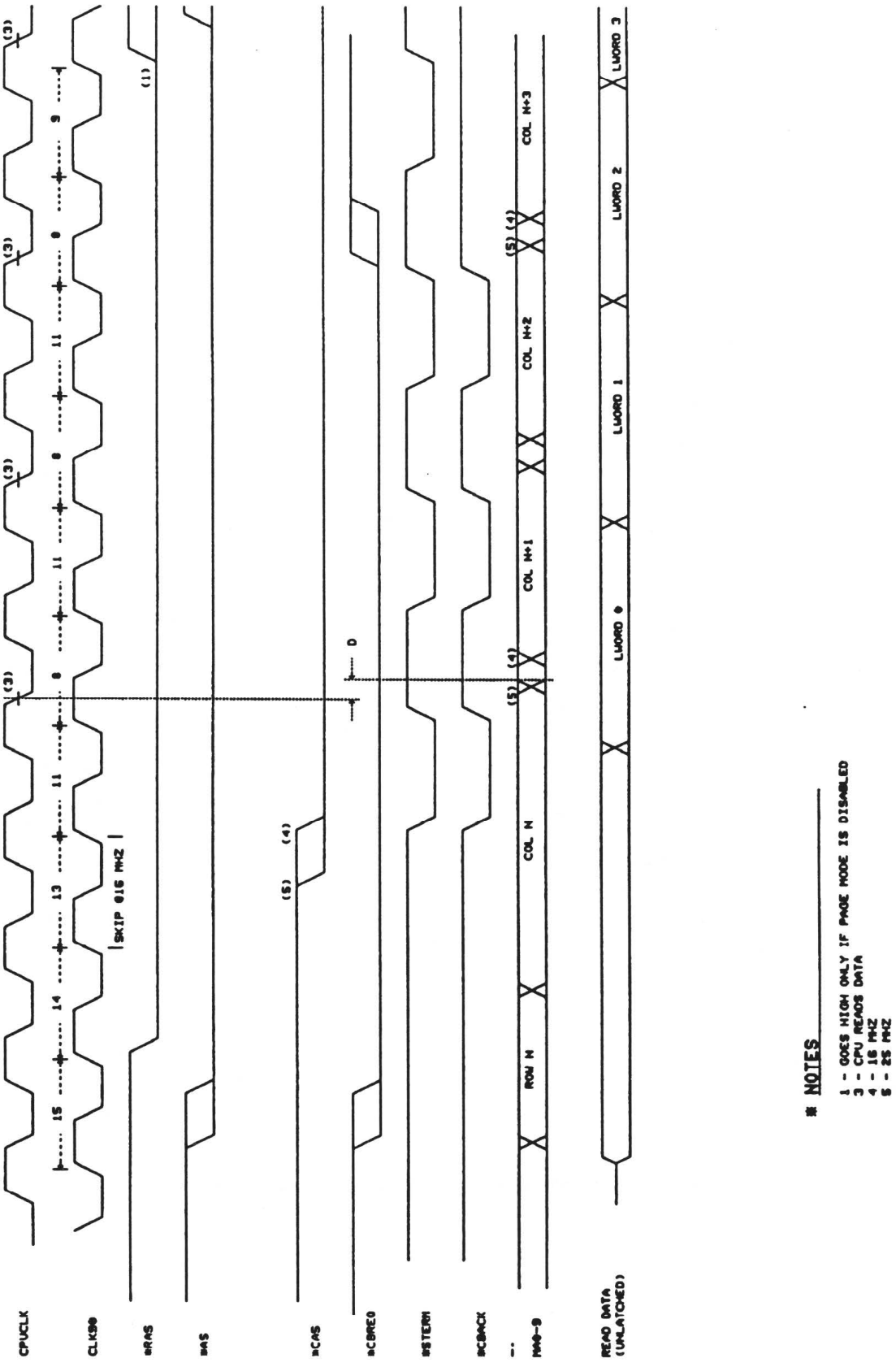

Figure 6-19. Burst Read Timing Diagram (No Page Was Open or Was Just Closed)

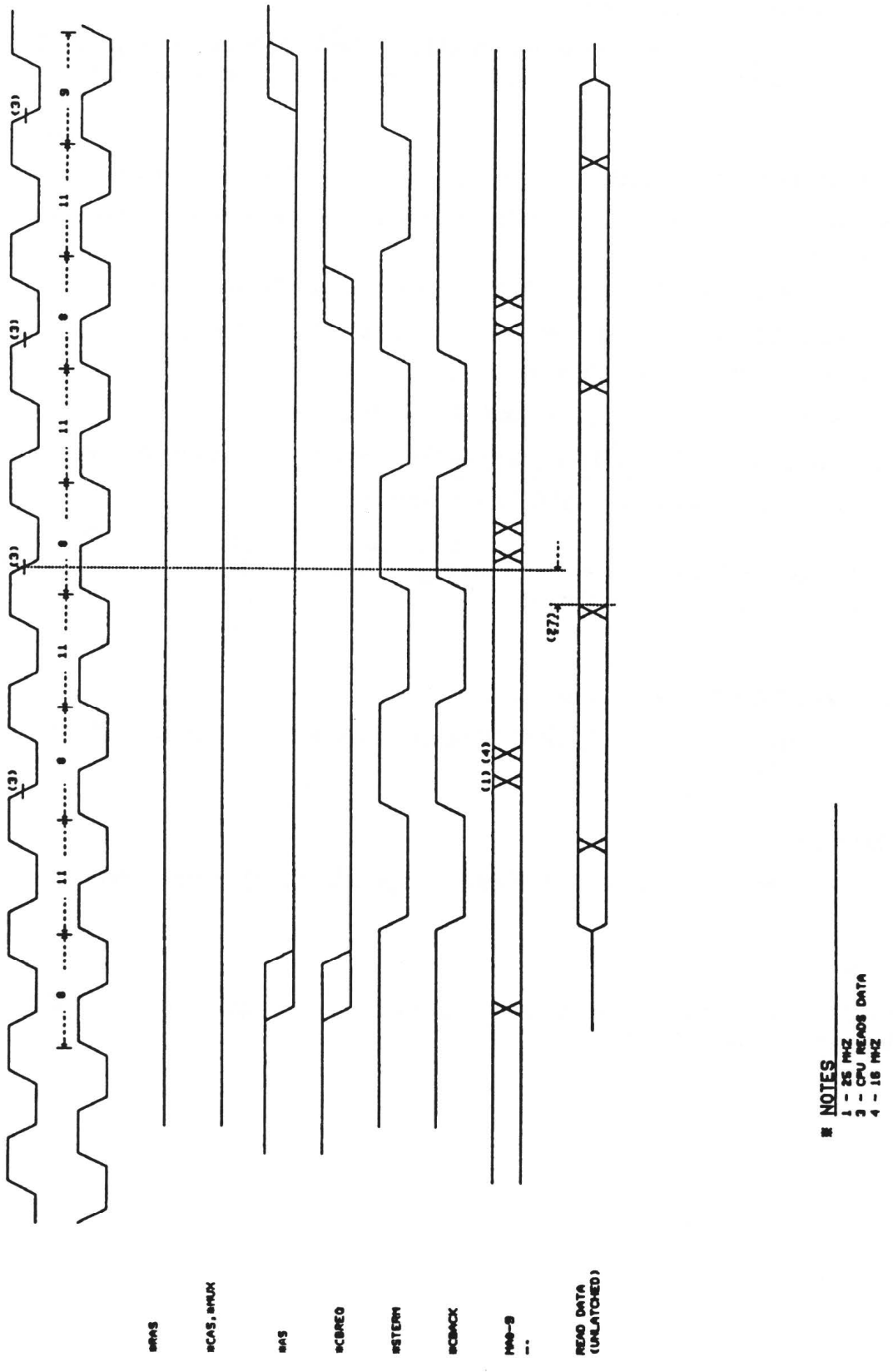

Figure 6-20. Burst Read (Page Hit)

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 85% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)

Note Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age Of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

Markings

Devices shall be marked with Commodore part number and copyright notice (© CBM 1989/90) and vendor part number (50012).